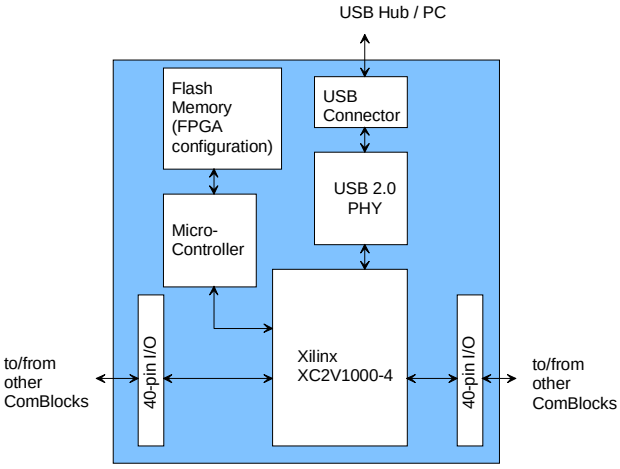
COM-1100
FPGA / VHDL DEVELOPMENT PLATFORM & USB 2.0 HIGH-SPEED INTERFACE

Key Features

- Develop custom signal processing applications on FPGA in VHDL language using this generic development platform.
- Xilinx Virtex-II XC2V1000-4 FPGA features 1 million system gates, 720Kbit of dual port memory, 40 18x18 multipliers.
- USB 2.0 peripheral interface for data transfers up to 448 Mbit/s.
- USB 2.0 interface supports signaling rates of 480 Mbits/s (High Speed) and 12 Mbits/s (Full Speed).
- Modules can be stacked for large VHDL design development.
- FPGA configuration remains in non-volatile flash memory and is automatically reloaded at power up.
- Graphical User Interface is used for remote monitoring and control over simple serial link. This includes loading FPGA configuration file into flash. No special cable nor serial EPROM is needed.
- This module is interface compatible with other pre-programmed ComBlock modules.
- Microprocessor automatically configures FPGA at power up.
- 200 MHz internal clock rate. External clock selection.
- Single 5V supply with reverse voltage and overvoltage protection. Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom).



Block Diagram

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com1100.pdf.
These specifications are subject to change without notice.

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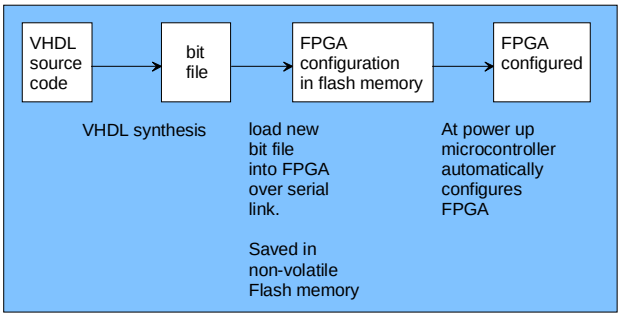
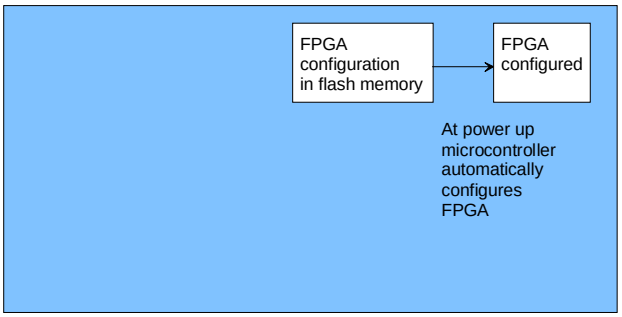
Application Development Process



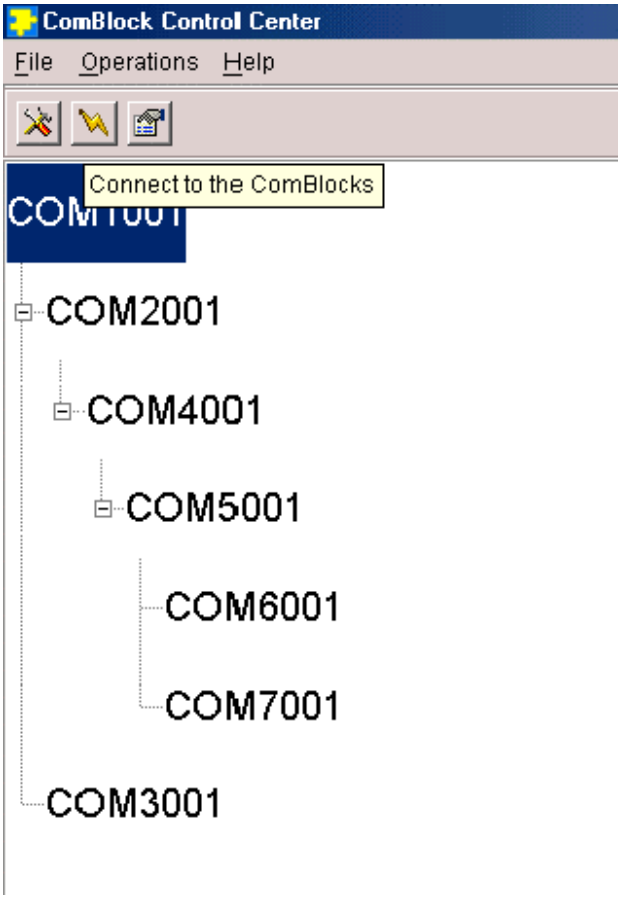
Development environment.



Run-time environment..

Graphical User Interface

When activated, the GUI enumerates the ComBlock modules within the assembly. The modules are identified by their name in a tree-like structure. Each module can be configured and monitored remotely.



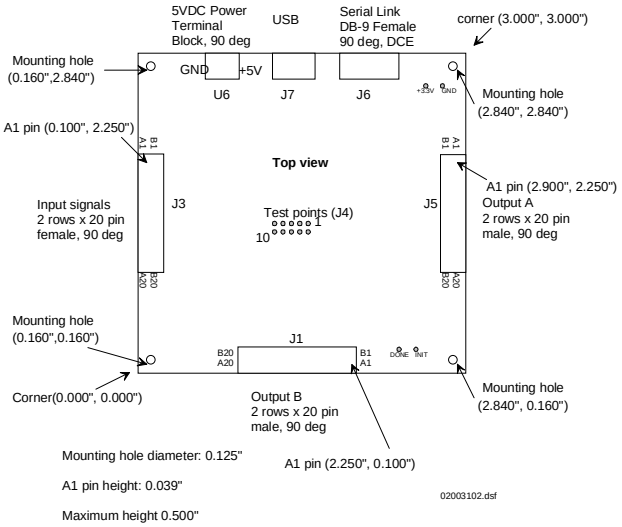
The ComBlock Control Center software is provided with all ComBlock modules. The user's manual can be found at
www.comblock.com/download/ccchelp.pdf

Electrical Interface

Interfaces	Definition
J3(34:1)	J3 connector (left). Mostly used for input signals.
J1(34:1)	J1 connector (bottom). Mostly used for output signals. J3(1) plays a special role as external clock, an alternative to the internal 40 MHz clock.
J5(34:1)	J5 connector (right). Mostly used for output signals.
TEST_POINTS(10:1)	Ten test points are provided in the form of a dual-row 0.1" spacing header for easy access by an oscilloscope probe.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to

	the CLK frequency. The maximum power consumption at 200 MHz is TBDmA.

Mechanical Interface



Schematics

The board schematics are available on-line at www.comblock.com/download/com_1100schematics.zip

VHDL code samples

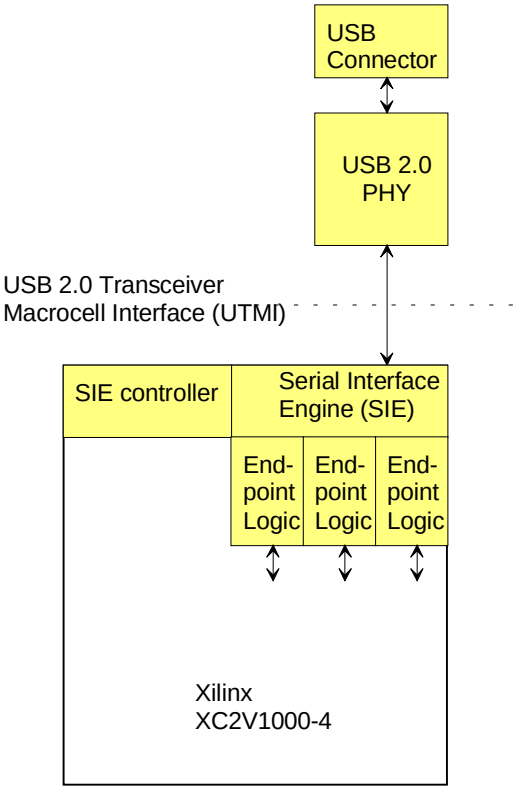
VHDL project samples are available on-line at TBD.

Each project includes:

- the VHDL source code (.vhd)
- the constraint file (.ucf) listing all pin assignments.
- The Xilinx project with the synthesis and implementation settings.
- The resulting bit file (.hex) ready to be loaded into flash memory.

USB peripheral implementation

The USB peripheral implementation is divided into two sections: a very high-speed physical layer, mostly analog, processing (USB transceiver macrocell), and a lower speed digital section comprising the serial interface engine (SIE), the SIE controller, and the end-point logic. The physical layer is implemented by a specific integrated circuit (SMSC GT3200) whereas the digital processing is implemented within the FPGA.



The interface between the FPGA and the USB 2.0 PHY transceiver is described by the "USB 2.0 Transceiver Macrocell Interface (UTMI) Specifications", Version 1.05 3/29/2001. It can be downloaded from www.usb.org

From its USB interface, the COM-1100 is a self-powered device: it does not draw power from the USB interface.

I/Os

Important: The I/O signals connected directly to the FPGA are NOT 5V tolerant!

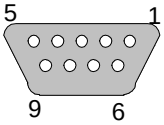
Pinout

USB

USB type B receptacle, as the COM-1100 is a USB device.

Serial Link

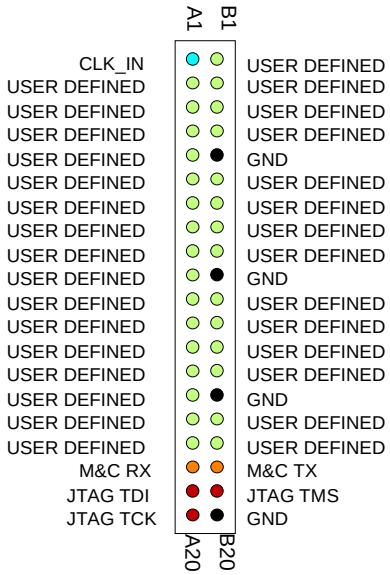
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



DB-9 Female

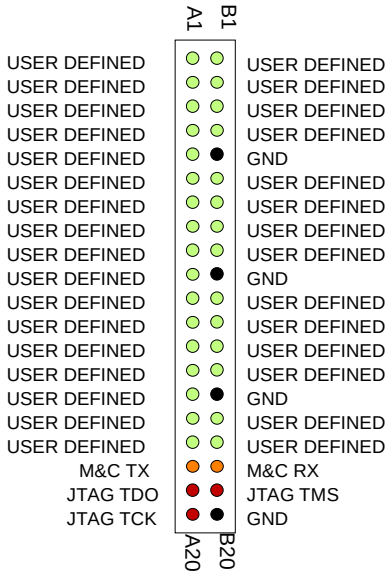
2 Transmit
3 Receive
5 Ground

(Input) Connector J3



Note: although the J3 connector is generally referred to as ‘Input’, individual user-defined pins can be configured as ‘IN’, ‘OUT’, or ‘INOUT’ in the user VHDL source code.

(Output) Connectors J1,J5



Note: although the J1/J5 connectors are generally referred to as ‘Output, individual user-defined pins can be configured as ‘IN’, ‘OUT’, or ‘INOUT’ in the user VHDL source code.

ComBlock Ordering Information

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